Y.Roji ,INDIA / International Journal of Research and Computational Technology,
Vol.8 Issue.2 *page: 01-08*
ISSN: 0975-5662, **July, 2016** **www.ijrct.org**

DESIGN OF LOW POWER 4-BIT CMOS COLUMN AND ROW BYPASS MULTIPLIERS

[1]Y.Roji [2]Dr.C.V.Krishna Reddy [3]Hemalatha [4]D.Lakshmaiah
[1]Assistant professor ,VBIT,Hyd . [2] professor of ECE Dept NNGI , Hyd .[3]professor ,OU .[4]Assso.prof,CJITS Hyd
laxmanrecw@gmail.com

ABSTRACT:

Power management has become a great concern in VLSI design in recent years. It is well know that multiplier consumes most of the power in Digital signal processing computations it is very important for modern Digital signal processing system to design low power multipliers to reduce power. This paper explores the design techniques of multiplier and aims to reduce power consumption. Here the bypassing techniques are used to reduce power consumption.Based on the simplification of the addition operations in a low-power bypassing-based multiplier, a low-cost low-power bypassing-based multiplier is proposed. In this paper Row-bypassing multiplier, column-bypassing multipliers are implemented by using the 90nm and 65nm technologies.

KEY WORDS:Power, Area, PDP(Power Delay Product), Full Adders.

SOFTWARE:MICROWIND version 2.

I. INTRODUCTION:

Multiplication is the basic building block for several DSP processors, Image processing and many other. Over the years the computational complexities of algorithms used in Digital Signal Processors (DSPs) have gradually increased. This requires a parallel array multiplier to achieve high execution speed or to meet the performance demands.[6]

In modern VLSI system, power is the most important parameter to optimize for low power applications like Digital Signal Processor (DSP), portable devices etc. DSP is one of core technologies for multimedia and mobile applications, most DSP applications entail addition and multiplication arithmetic operations. Especially, the multiplier is the critical arithmetic operation unit for many DSP applications, such as filtering, convolution, Fast Fourier Transform (FFT), etc. Analysis of the conventional DSP applications shows that the average of zero input of operand in multiplier is 73.8 percent. An important low power design to reduce power consumption is to shutdown part of a circuit while it is not in operation. The power reduction in multipliers can be achieved using bypassing technique in DSP's [6].

Multipliers have large area, long latency and consume considerable power. Therefore, low power multiplier design has been an important part in low-power VLSI system design.

Power dissipation:

CMOS is currently the dominant technology in digital VLSI. Two components contribute to the power dissipation in CMOS circuits. The static dissipation is due to leakage current, while dynamic power dissipation is due to switching transient current as well as charging and discharging of load capacitances. Since the amount of leakage current is usually small, the major source of power dissipation in CMOS circuits is the dynamic power dissipation.

Dynamic power dissipation appears only when a CMOS gate switches from one stable state to another. Thus, the power consumption can be reduced if one can reduce the switching activity of a given logic circuit without changing its function.[7]The power dissipation in CMOS circuit [8]is given by,

$$P = (1/2)*C*V2*f*N,$$

Where,
P is the power dissipation,
C is the load capacitance,
V is the supply voltage,
f is the frequency of the clock,
N is the total number of switching activities in one clock cycle.

Dynamic power is due to the switching activities. So, by reducing the switching activity thedynamic power can be reduced.

II. LITERATURE SURVEY:

Yin-TsungHwang ,Jin-Fa Lin ,Ming-HwaSheu and Chia-Jen Sheu [1] Proposed two novel low power multipliers circuits based on enhanced row bypassing schemes. The essence of the power saving idea is eliminating unnecessary computation via signal bypassing**.** For a low-power row-bypassing multiplier, the addition operations in the j-th row can be disabled to reduce the power dissipation if the bit bj in the multiplier is 0, i. e., all partial products aibj, $0 \leq i \leq n-1$, are zero. As a result, the addition operations in the jth row of CSAs can be bypassed and the outputs from the (j-1)-th row of CSAs can be directly fed to the (j+1)-th row of CSAs without affecting the multiplication result.[9]

Tushar V. More and Dr. R.V.Kshirsagar [2] Presented a low power column bypass multiplier design methodology that inserts more number of zeros in the multiplicand thereby reducing the number of switching activities as well as power consumption. The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated. If multiplicand contains more zeros, higher power reduction can be achieved. Further low power adder structure reduces the switching activity.

Ugurdag,F.Keskin.O,TuncC,Temizkan.F ,Fici,G,Dedeoglu, S [4]Proposed a high-performance hardware design, employing the component level optimizations for building fast multipliers. Most of the fast multiplier architectures uses some form of Carry Save Adder (CSA) Tree, which is also called Column Compression (CC). They proposed a new method called RoCoCo (Row and Column Compression), which also compresses the tree along rows so that the final adder is small and fast. Although CC results in faster multipliers in ASIC implementations, it is an assumption by designers that they are not the wisest choice on FPGAs. On the contrary, they were able to show through Xilinx synthesis results that RoCoCo frequently offer faster multipliers than the built-in implementation of the multiply operation in Xilinx ISE synthesis tool.

Gang-Neng Sung, Yan-JhihCiou, and Chua-Chin Wang[5] Presents a low power digital multiplier design by taking advantage of a 2-dimensional bypassing method in cell-based design flow. The proposed bypassing cells constituting the multiplier skip redundant signal transitions when the horizontally partial product or the vertically operand is zero. Thorough cell-based design flow post-layout simulations show that the power delay product of the proposed 8×8 multiplier design is reduced by more than 13.8% compared to prior designs. It justifies the advantage in terms of power delay product after the software optimization.

Nan-Ying Shen et al (2012) presented Low-power 2's complement multipliers are developed through minimizing switching activities of partial products using the radix-4 Booth algorithm. Before computation, the input datum with the smaller effective dynamic range is processed to generate Booth codes, thereby increasing probabilities of partial products being zero. By employing the dynamic-range determination units to control input data paths, the proposed 16×16-bit multipliers based on the Yu, Goldovsky, and Mahant-Shetti's low-power approaches are individually implemented. It illustrates the proposed multiplier having low-power dissipation; the theoretical analyses of switching activities of partial products are derived. Compared to the power consumed by the conventional multipliers. The proposed multipliers conserve more than 14%, 30% and 31% of power, respectively.

More &Kshirsagar (2011) presented low power Column bypass multiplier design methodology that inserts more number of zeros in the multiplicand thereby reducing the number of switching activities as well as power consumption. The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bitcoefficient is zero, corresponding row or column of adders need not be activated. If multiplicand contains more zeros, higher power reduction can be achieved. To reduce the switching activity is to shut down the idle part of the circuit, which is not in operating condition. Use of look up table is an added feature to this design. Further, low power adder structure reduces the switching activity. Flexibility is another critical requirement that mandates the use of programmable components like FPGAs in such devices.

III. PROPOSED WORK:

1.1 BIT CMOS FULL ADDER

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin; 'A' and 'B' are the operands, and Cin is a bit carried in (in theory from a past addition). The circuit produces a two-bit output sum typically represented by the signals Cout and S. Full-adders can be cascaded to build a multi-bit binary adder.

For the implementation of logic expression of eq1 and eq2, the full adder was designed with the help of 11MOS transistors. NOR-I, XNOR-II, and MUX are the three modules of 1-bit full adder. By considering two inputs and one output, XNOR-I and XNOR-II modules were designed by using 5MOS transistors.

For optimum operation, the MUX module is designed with the help of two MOS transistors. The implantations of full adders are shown in fig. 6MOS transistors were combined with XNOR and XOR logic. MUX logic with 2MOS transistors for optimum operation. Implementation of full adder with 11MOS transistors is shown in fig.

$$SUM = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + ABC_{in} \ldots (1)$$

$$CARRY = AB + AC_{IN} + BC_{IN} \ldots (2)$$

CMOS FULL ADDER CIRCUIT:

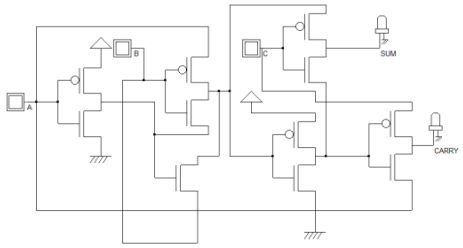


Fig1: CMOS Full Adder

2. 1 BIT CMOS HALF ADDER:

Half adder is acombinational logic circuit with two inputs and two outputs. It is the basic building block for addition of two single bit numbers. Two one-bit binary numbers A and B is added by the half adder. It has two outputs namely "carry" and "sum".

$$SUM = A\bar{B} + \bar{A}B$$

$$CARRY = AB$$

The half-adder design incorporates an XOR gate for S and anAND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The operational truth table of half adder is shown in table where A, B are the inputs and sum and carry are the outputs of half adder while its schematic shown in figure.

CMOS HALF ADDER CIRCUIT:

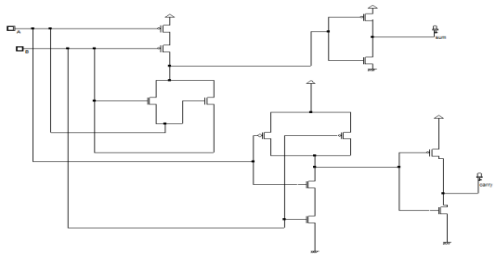


Fig2**:** CMOS Half adder circuit

3. 2 TO 1 MULTIPLEXER

A multiplexer (or mux) is a common digital circuit used to mix a lot of signals into just one. If you want multiple sources of data to share a single, common data line, you'd use a multiplexer to run them into that line. Multiplexers come in all sorts of shapes and sizes, but they're all made out of logic gates.

Every multiplexer has at least one select line, which is used to select which input signal gets relayed to the output. In a 2to1 multiplexer, there's just one select line. More inputs means more select lines: a 4to1 multiplexer would have 2 select lines, an 8to1 has 3, and so on (2 inputs require *n* select lines). Think of a mux as a "digital switch". The select line is the throw on the switch, it chooses which of the many inputs get to be the output.

CMOS CIRCUIT

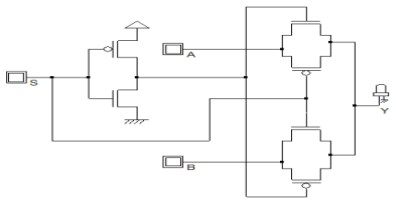


Fig3: CMOS circuit of 2 to 1 multiplexer

4. BYPASSING MULTIPLIERS:

- COLUMN BYPASS MULTIPLIER
- ROW BYPASS MULTIPLIER

4.1 COLUMN BYPASS MULTIPLIER

While designing the circuit for column-bypassing multiplier, it is essential to set the carry outputs to 0 in the bottom of the CSA array, otherwise, the corresponding FA's may not produce the correct outputs since their inputs are disabled. This is done by adding an AND gate at the outputs of the last-row CSA adders as shown in the following circuit diagram of Column bypassing multiplier.

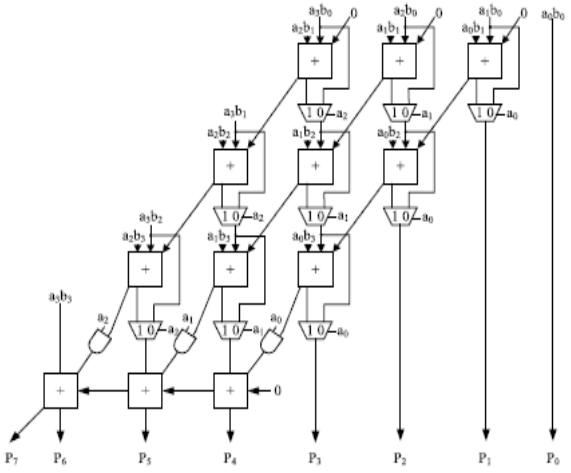


Fig4: Column bypass multiplier architecture

The design of any multiplier completely depends on the internal structure of the adder cell. In column-bypassing multiplier the internal structure of the adder cell is designed in the manner that it is capable of by-passing certain columns, whenever it detects the corresponding bits of multiplicand to be zero.

It uses additional two Tri-state buffers and one multiplexer, compared to Standard Braun's multiplier, in its internal adder structure to bypass a column.

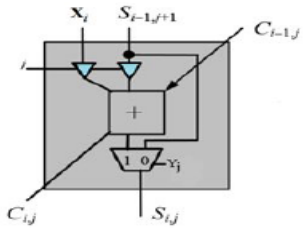


Fig5: Column bypass multiplier adder cell

An important point to be noted here is that, the input carry bit (Ci–1,j) does not enter the adder cell through Tri-state buffer. It is so because, for a Braun's multiplier, there are only two inputs for each FA in the first row (i.e., row 0), when Yj = 0, the two input of FA0,j are disabled, and thus its output carry bit will not be changed. Therefore, all three inputs of FA1,j are fixed, which prohibit its output from changing.

4.2 ROW BYPASS MULTIPLIER

This is a modified version of Braun's multiplier which is a parallel multiplier and contains adders in array form. In this method transition activity optimization is achieved through bypassing row of adders which are redundant. It's known that in multipliers, partial products are created by AND ing the multiplicand bits with the multiplier bits one by one.

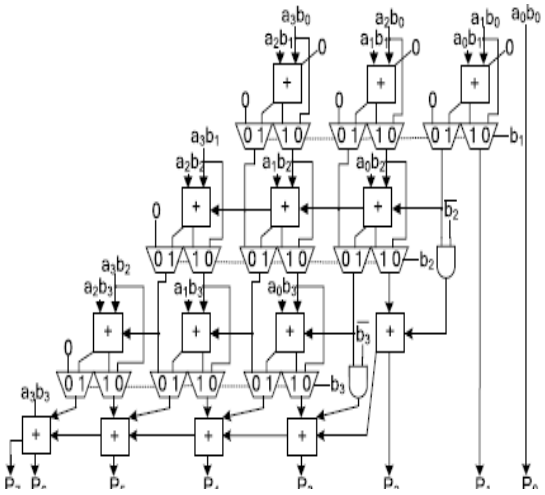


Fig6: Row bypassmultlier architecture

It is always possible that a bit in the multiplier is a zero, in this case, as the zero bit enters as one of the input of the AND gate to produce a partial product, zero being the dominating factor, forces the output to be zero, this means that the complete row of partial product becomes zero. Now adding elements of this row, in adder circuit present in the array of full adders is merely wastage of energy, as adding a zero bit yields the same output as it was before adding it. So, in this multiplier circuit it is proposed to dynamically bypass such additions by disabling the complete row of adders, thus decreasing the number of signal transitions in the carry-adder array without affecting the result.

Whenever it's detected that the select line is zero, the output of the previous adder is passed through the multiplexer to the input of the next adder, and in the same time the partial product is interrupted to enter the adder circuit with the help of Tri-state buffer present in the input. Thereby results in bypassing the complete row of adders.

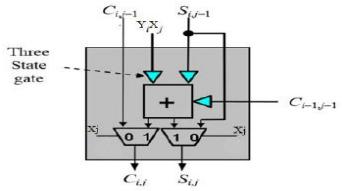


Fig7: Adder cell of row bypass multiplier

IV.PERFORMANCE AND SIMULATION RESULTS

COLUMN BYPASS MULTIPLIER DESIGN

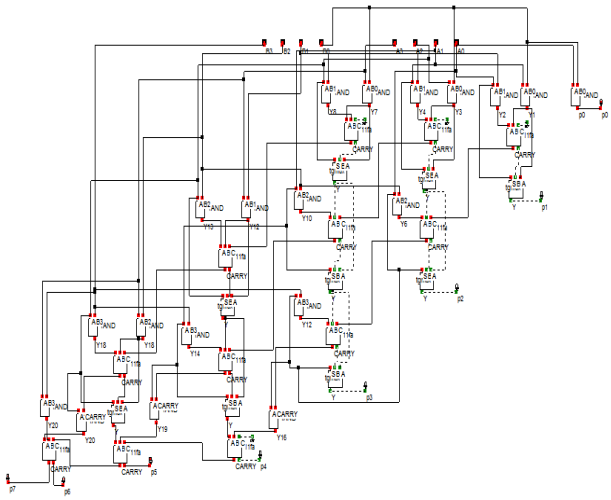


Fig8: Design of columnbypass multiplier

Simulation

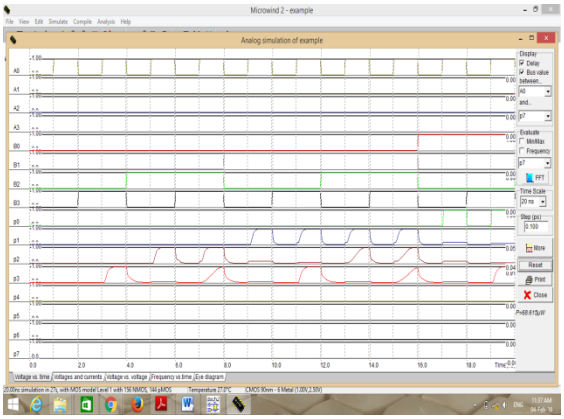


Fig 9: simulation of column bypass multiplier

RESULT OF COLUMN BYPASS MULTIPLIER:

At 27˚C

TECHNOLOGY	POWER (µw)	AREA (µm)	Delay(ns)	PDP (PJ)
Cmos 90nm	68.615	201.05	12.550	0.861

Cmos 65nm	22.106	98.66	12.550	0.27

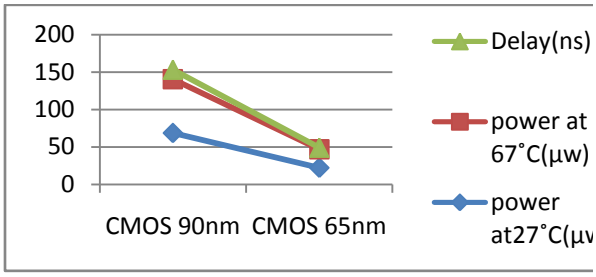
Table 1: column bypass multiplier power report at27˚C

At 67˚C

TECHNOLOGY	POWER (µw)	AREA (µm)	Delay (ns)	PDP (PJ)
Cmos 90nm	71.877	109.485	12.550	0.902
Cmos 65nm	24.878	53.816	12.550	0.312

Table 2: Row bypass multiplier power report at27˚C

Comparisionof power and delay of column multiplier at different temparatures



ROW BYPASS MULTIPLIER DESIGN

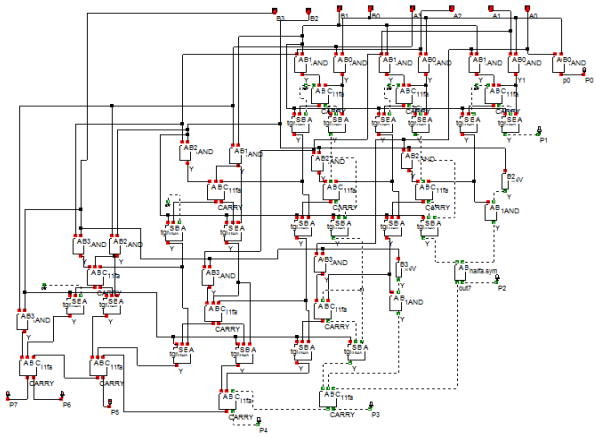


Fig10: Design of row bypass multiplier Simulation

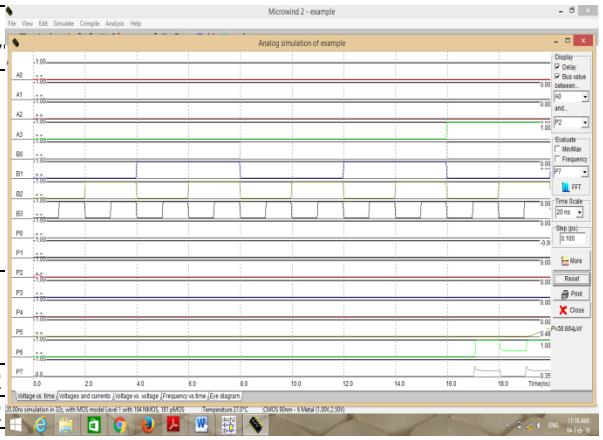


Fig11: simulation of row bypassmultiplier

RESULTS OF ROW BYPASS MULTIPLIER

At 27˚C

TECHNOLOGY	POWER (µw)	AREA (µm)	Delay (ns)	PDP (pJ)
Cmos 90nm	58.684	319.41	14.55	0.853
Cmos 65nm	17.719	78.264	14.55	0.257

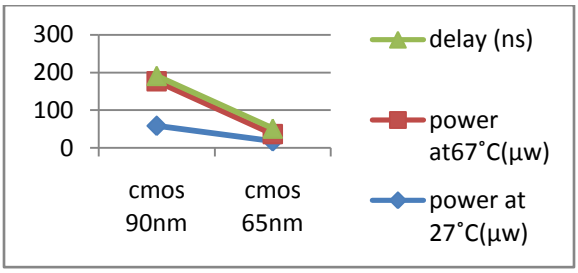
Table 3: Row bypass multiplier power report at 27˚c

At 67˚C

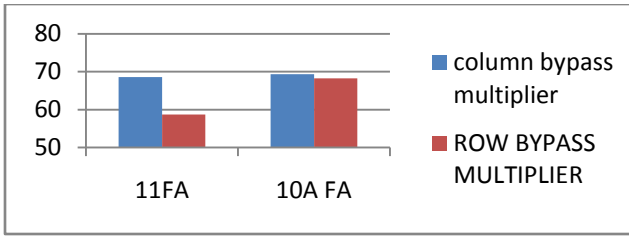
TECHNOLOGHY	Power (µw)	Area (µm)	Delay (ns)	PDP (pJ)
Cmos 90nm	118	503.14	14.55	1.716
Cmos 65nm	19.349	89.29	14.55	0.281

Table 4: Row bypass multiplier power report at 67˚C

Comparisionof power and delay of rowbypassMultiplier at different temparatures:



comparision of power dissipation in column and row bypass multipliers



Comparision of power dissipation in proposed and existing work:

Types of multipliers	Proposed work Power(µw)	Existing work Power(µw)
Column bypass multiplier	68.615	208.9
Row bypass multiplier	58.684	187.7

Table5: power dissipation for different multipliers

V. CONCLUSION:

In this paper we designed column and row bypass multipliers by using MICROWIND TOOL. Row bypass multiplier has more circuitry compared to column bypass multiplier. The power dissipation of column bypass multiplier is 68.615(µw) and row bypass multiplier power dissipation is 58.684(µw). Row bypass multiplier has less power dissipation than column bypass multiplier but the disadvantage is more delay. Thus we conclude that column bypass gives least delay and row bypassing gives least dissipation.

VI. Future Scope :

The present work on new multiplier architecture can be extended in various directions. Based on the initial study, and the understanding established, the following suggestions are proposed suggestions:

- To implement the row and column bypassing technique on different tree algorithms.
- To focus on both, generation as well as accumulation stage.

ACKNOWLEDGEMENT

REFERENCES

1. Y.T.Hwang , J.F. Lin ,M.H Sheu and C.J Sheu "Low-Power Multiplier Design with Row and Column Bypassing", in *Proc. IEEE International SOC Conference (SOCC 2009)* , June2005, PP. .345-349.
2. T. V. More and Dr. R.V.Kshirsagar "Design of Low Power Column Bypass Multiplier using FPGA", in *Proc. IEEE International Conference on Electronics Computer Technology (ICECT)*, 2011 ,Vol.3 , PP. 431 - 435.
3. J.T. Yan and Z.W Chen, "Low-Power Multiplier Design with Row and Column Bypassing," in *Proc. IEEE SOC Conference (SOCC 2009*), June 2002, PP.1227-230
4. Ugurdag , F.Keskin.O,TuncC,Temizkan.F,Fici,G,Dedeoglu, "RoCoCo: Row and Column Compression for high-performance multiplication on FPGAs"in*Proc. 2011 9th East - West Design and Test Symposium,(EWDTS)* ,2011,PP. 839-844.
5. G.N.Sung, Y.J.Ciou, C.C.Wang, "A power aware 2-dimensional bypassing multiplier using cell – based design flow", *in Proc. IEEE International Symposium on Circuits and Systems (ISCAS 2008)*, May 2008, pp. 3338 – 3341.
6. Anitha R, Bagyaveereswaran V ,"Braun Multiplier Implementation using FPGA with BypassingTechniques", International Journal

of VLSI design & Communication Systems (VLSICS) Vol.2,.

7. M. C. Wen, S. J. Wang and Y. M. Lin," Low power parallel multiplier with column bypassing".
8. Neil H. E. Weste, David Harris and Ayan,CMOS VLSI Design (pearsoneducation Asia, third edition, 2006