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Design of High speed Low-Power 1-Bit CMOS Full Adder using FPGA Kit and Microwind.3

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*Abstract:-**The aim of the paper is to implement a 14T Full adder cell, that utilize low power by using XOR and XNOR gate architectures with pass transistor logic and transmission gate. It has been developed for low power consumption by reducing the number of transistor. The power consumption can be reduced by 50% using proposed full adder compared with convectional full adder. All simulation results have been carried out by using Micro wind 3.1 Tool based on 32 nm CMOS technology at 1.2 V supply voltages and Xilinx 13.2 suite. The simulation results of 1-bit adder cell proposed full adder shows that the proposed full adder has low power consumption and power delay product of SUM and COUT. The hardware implementation of 14T full adder is carried on Spartan 3e kit.***

Keywords:-Full Adder, XOR, XNOR, FPGA Kit

I. INTRODUCTION.

In very large scale integration (VLSI) systems, full adder circuit is used in arithmetic operations for addition, multipliers and Arithmetic Logic Unit (ALU). It is a building block of the application of VLSI, digital signal processing, image processing and micro processors. Most of full adder systems are considered performance of circuits, number of transistor, speed of circuit, chip area, threshold loss and full swing output and the most important is power consumption. In the future, portable devices such as cell phone, laptop computer, tablet etc. that need a low power and high speed for components are requirements. For this reason, design of low power is the research problems. In the paper is proposed I-bit full adder base on 22 nm CMOS technology which operation for low supply voltage is 1.2V at 250 MHz

2. PROPOSED WORK.

14 Full Adders

The top module of 14T full adder cleverly hides implementation complexity of 14T full adder. The inputs of 14T full adder top order are A, B, Cin and where as outputs are SUM, COUT. Top order module consists three inner modules, better interfacing is providing between the modules. The following figure 1 shows the flow diagram of 14T full adder.

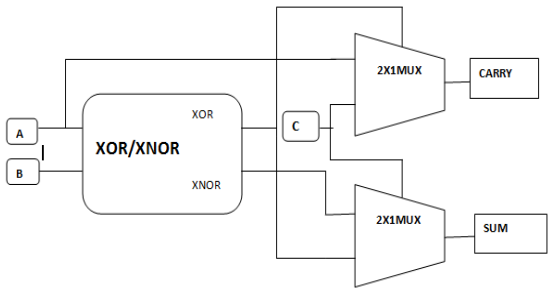

Figure (1) 14 Transistor 1 bit Full Adder Block Diagram

A 14 transistor full adder was designed based on reduction of power and area. The full adder consists four modules, XNOR-I, XOR-I and MUX -I and MUX-II. The XNOR and XOR logic is combined with 6 MOS transistors and MUX logic with 2 MOS transistors for optimum operation. The implementation of full adder with 14 MOS transistors is shown in fig. 1and 3.

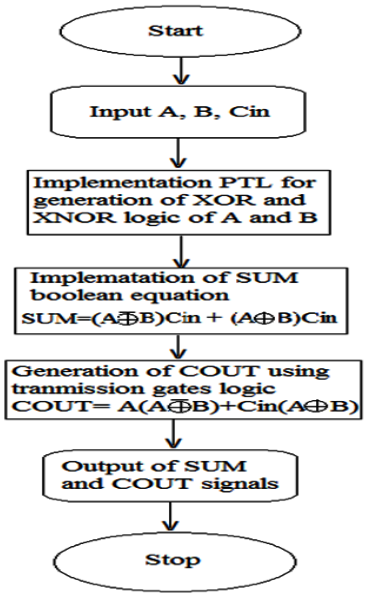

Fig 2: Flow Chart of Top order module

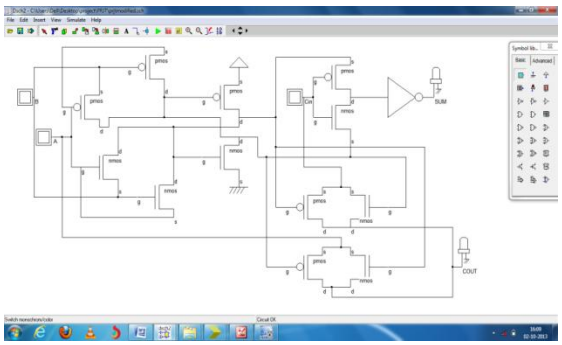

Figure (3) 14 MOS Transistor 1 bit-CMOS Full Adder circuit.

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing, hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/Os and bidirectional data buses it becomes a challenge to verify correct timing of valid data within setup time and hold time. Floor planning enables resources allocation within FPGA to meet these time constraints.

For the hardware implementation of 14T full adder FPGA Spartan 3e kit is used. The features of spartan3e are listed below.

3. PERFORMANCE AND SIMULATION RESULTS:-

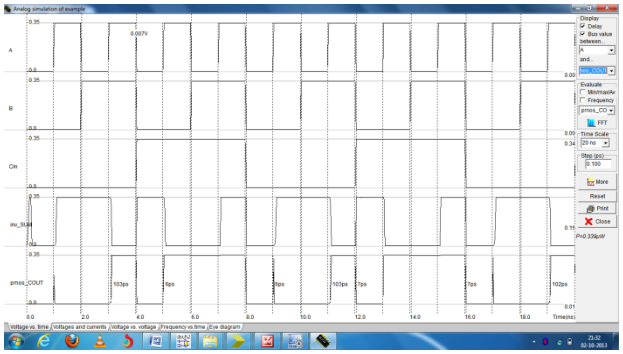

Fig (4): Simulation Results of14 CMOS Full Adder top module in Micro wind

The simulation results of top order module in Micro wind simulation environment using 32nm technology as shown in fig (4)

Parameters	14T full adder
Area	0.348sq-nm
Power consumption	0.339µw
Time Delay	0.95ns
Power Delay Product	0.322(µw×ns)

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Table 1: Simulation results of 14T full adder Micro wind Tool

FULL ADDER USING FPGA KIT:-

Synthesis Report provides a summary and analysis of net list generation, including a summary of your synthesis options. After design is created, the design

files are synthesized. The synthesis process checks code syntax analyzes the hierarchy of your design, recognizes the functionality described, and ensures that your design is optimized for the device architecture you selected. The resulting netlist is saved to an NGC file for Xilinx Synthesis Technology (XST) or to an EDIF file for Precision, simplify, or simplify Pro synthesis tools. The figure 5 shows the synthesis tool in Xilinx environment.

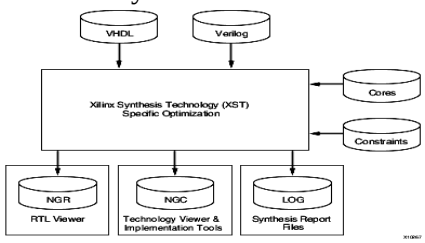
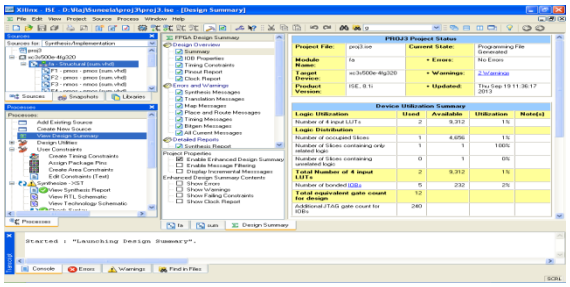
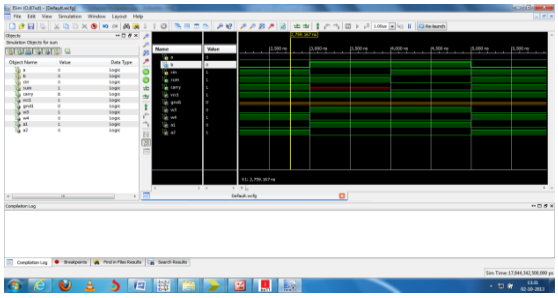


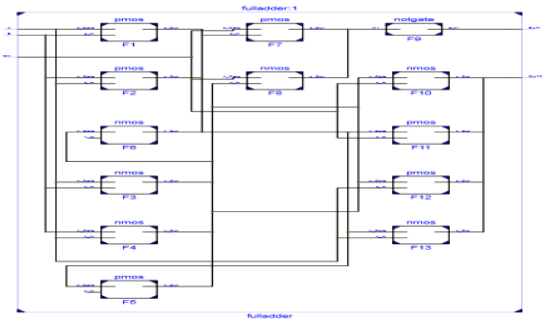
Fig (5): Synthesis tool in Xilinx environment



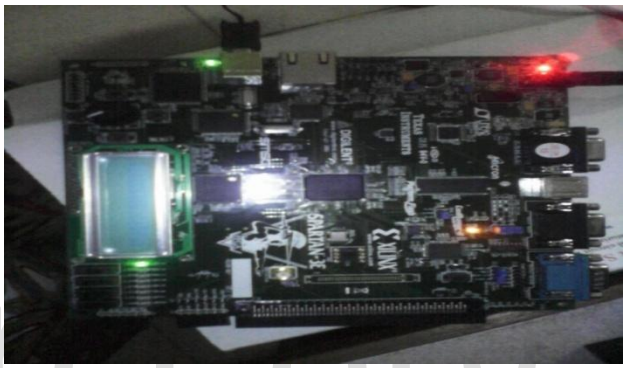
Fig(6) Synthesis Report



Fig(7).Full Adder Xilinx simulation result



Fig(8).Full Adder RTL Circuit diagram



Fig(9).FPGA Kit

CONCULTION:-

The modular way of implementation of 1- bit 14T full adder is done, simulated using Micro wind tool and Xilinx tool. This is suitable for 1.2v voltage supply applications. The arithmetic and logical unit is constructed using 1-bit 14T full adder circuit. The proposed circuit improves the performance of speed and driving capability because it has full out voltage swing. The parameters like area, time delay, power consumption are calculated and compared with conventional full adder. The hardware implementation is carried of FPGA Spartan 3e kit.

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